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Substitute for form 1449/PTO **SUPPLEMENTAL** INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet

(Use as many sheets as necessary)

Complete if Known				
Application Number	10/684,713			
Filing Date	10/14/2003			
First Named Inventor	Paul Arthur Layman			
Art Unit	2811			
Examiner Name	Unassigned			
Attorney Docket Number	Chaudhay 25, 18, 8, 12, 5/075003, 282			

			U. S. PATENT	DOCUMENTS	
Examiner Initials*	Cite No.1	Document Number Number-Kind Code ^{2 (8 known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
RP	Α	us- 6475866	11-05-2002	Hofmann, et al	
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Examiner Initials*	Cite No.1	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages	_
		Country Code ³ Number ⁴ Kind Code ⁸ (if known)	MM-DD-YYYY	· · · · · · · · · · · · · · · · · · ·	Or Relevant Figures Appear	T
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Examiner Date

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Substitut	te for form 1449/PTO			Complete if Known		
	SUPPLEMENTAL		Application Number	10/684,713		
INFO	INFORMATION DISCLOSURE STATEMENT BY APPLICANT			Filing Date	10/14/2003	
STA				First Named Inventor	Paul Arthur Layman	
	(i lea se manu che	ante ac n	araocand	Art Unit	2811	
	(Use as many sheets as necessary)			Examiner Name	Unassigned	
Sheet	2	of	2	Attorney Docket Number	Chaudhry 25-18-8-12-5/075903-282	

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
RP	1	DUDEK, ET AL, "Lithography-Independent Nanometer Silicon MOSFET's on Insulator", IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1626-1631.	
RP	2	RISCH, ET AL, "Vertical MOS Transistors with 70 nm Channel Length", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498.	·
RP	3	TAKATO, ET AL, "Impact of Surrounding Gate Transistor (SGT) for Ultra-High-Density LSI's", IEEE Transactions on Electron Devices, Vol. 38, No. 3, March 1991, pp. 573-577.	
RP	4	TAKATO, ET AL, "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs", IEDM 1988, pp. 222-225.	
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		HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFETt: A High Performance Vertical MOSFET with Lithography-Independent Critical Dimensions", no publication information apparent from document.	
RI	8	MONROE, ET AL, "The Vertical Replacement-Gate (VRG) Process for Scalable, General-purpose Complementary Logic", Paper 7.5, pp. 1-7, date and publication information unknown.	

Examiner Signature	ompey	Date Considered	6-28-13

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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18
Stylesheet Version v18.0

Title of Invention Multiple Operating Voltage Vertical Replacement-Gate (VRG) Transistor

Application Number:

10/684713

Confirmation Number:

4836

First Named Applicant: Paul Layman Attorney Docket Number: 075903-282

Art Unit:

2811

Search string:

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or 5554870 or 5864158 or 6268621).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
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	2	5010386	1991-04-23	Groover, III			
	3	5140388	1992-08-18	Bartelink			
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Signature

Examiner Name	Date
Ron Pompey	6-28\$05